## REMARKS

A total of 51 claims remain in the present application. The foregoing amendments are presented in response to the Office Action mailed August 30, 2005, wherefore reconsideration of this application is requested.

By way of the above-noted amendments, claims 1, 19 and 39 have been amended to more clearly define features of the present invention. More particularly, claim 1 has been amended to explicitly define "a switch circuit adapted to select one of the master strobe signal and the local strobe signal". Similar amendments have been effected in claims 19 and 39. Claims 15, 35 and 51 have been amended to reflect the revisions effected in claims 1, 19 and 39, respectively. Claim 52 has been cancelled. Clearly, no new subject matter has been introduced.

Referring now to the text of the Office Action:

- claims 1, 2, 4-9, 16-23, 25-30, 36-44 and 52 stand rejected under 35 U.S.C. § 102(b), as being unpatentable over the teaching of United States Patent No. 5,257,261 (Parruck et al);

- claims 3 and 34 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent No. 5, 257,261 (Parruck et al) in view of United States Patent No. 6,160, 819 (Partridge et al.) and

- claims 10-15, 31-35 and 45-51 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As an initial matter, applicant appreciates the Examiner's indication of allowable subject matter in claims 10-15, 31-35 and 45-51. The Examiners claim rejections are believed to be traversed by the above-noted claim amendments, and further in view of the following discussion.

Rejections under 35 U.S.C. § 102(b)

With reference to claims 1, 19-22, 39-41 and 52, the Examiner has asserted (in part) that Parruck teaches a channel processor comprising " ... d) an output timer (e.g.

retiming block 18 in FIG. 1d) adapted to control a position of a read pointer (e.g. via pointer recalculation, see FIG. 1d and col. 5, line 35-col 7, line 21) for outgoing bits of the respective first data stream (e.g. STS-3#2) based on a selected one of the local (e.g. comprising J1 byte) and master (e.g., comprising control signal and B3 parity value) strobe signals (e.g. see col. 5, line 66 – col. 6, line 47)." With respect, Applicant believes that this interpretation is unsupported by the teaching of the Parruck reference.

Col. 5, line 35-col 7, line 21 describe operation of the retiming and pointer calculation block 18 of FIG. 1d. Thus:

> "the retiming and pointer recalculation block takes the incoming signal at the incoming STS-3 rate, demultiplexes the signal into three STS-1 type components, calculates new pointers (e.g., H1H2) for each STS-1 type signal, stuffs and destuffs the STS-1 signals as appropriate (in bytes H3 as seen in FIG. 6b and the first byte after the H3 byte--hereinafter referred to as byte0), and multiplexes the three STS-1 signals back into a retimed STS-3 type signal for output at the terminal side clock rate." (col 6, lines 8-17)

> "Turning to FIG. 2, details of the retiming and pointer calculation block 18 (and 30) are seen. In particular, the retiming apparatus of the invention includes a demultiplexer 40 for demultiplexing an incoming STS-3 type signal into three STS-1 type signals, three FIFOs 45-1, 45-2, and 45-3 for receiving the STS-1 signals, three depth measurement blocks 48-1, 48-2, and 48-3 for measuring the amount of data in the FIFOs, three frame counters 50-1, 50-2, 50-3 for counting the number of frames of data that have been demultiplexed since a pointer movement, logic decision block 52 for generating pointer movement (increments and decrements) based on the amount of data in each of the FIFOs, a pointer calculation block 54 for generating the pointers in response to information from logic decision block 52, and a multiplexer 55 for multiplexing the SPE data from each of the FIFOs, the pointer information as recalculated by the pointer calculation block 54, as well as other TOH data which may be either "dummy" information (i.e., all zeros), or data obtained from the RAM (of FIG. 1d)." [col 6, lines 48-68, underlining added)

> The H1 and H2 bytes of the TOH which point to the start of the SPE are generated by the pointer calculation block 54 based on information received by the logic decision block 52 [col 8, lines 52-57]
>
> "Turning to FIG. 3, a flow chart of the logic decision block 52 for an STS-3 signal is seen. The function of the logic decision block 52 is to determine when a stuff or destuff is needed, as well as to generate a control signal which will cause the stuff or destuff to be effected. Another function of the logic decision block 52 is to generate the stuff and destuff control signals in a manner which limits jitter. As previously described, the inputs to the logic decision block include the frame count(s) and the depth measurements." [col 9, lines 24-33]

Based on the foregoing, it will be seen that the "pointer recalculation" function referred to by the Examiner relates to the calculation of the H1H2 pointers of the outgoing STS frame, and the associated stuff and destuff decisions. More particularly, the logic decision block 52 receives the frame count and FIFO depth measurement (see fig 2, blocks 48-1 and 50-1, for example; and FIG. 3) and "determines when a stuff or destuff is needed, as well as to generate a control signal which will cause the stuff or destuff to be effected." The pointer calculation block 54 uses the information obtained from the logic decision block 52 to calculate the H1 and H2 bytes.

The person of ordinary skill in the art will instantly recognise that this operation is entirely related to the calculation of the SONET pointers, and more particularly the H1 and H2 payload pointers of the Transport Overhead. Furthermore, the person of ordinary skill in the art will instantly recognise that this has nothing what-so-ever to do with a "read pointer for reading buffered bits", much less controlling a position of the read pointer, as suggested by the Examiner.

In fact, Parruck describes at length his realignment mechanism at col. 11, line 60 through col. 13, line 68, and with reference to FIGs. 5a-c. In particular, FIG. 5a shows the logical circuit used to generate the FIFO read signals (READ#1, READ#2 and READ#3) used to read data out of each FIFO 45 (see FIG. 2). As can be seen from FIGs. 2 and 5a-5c, each of the FIFO read signals are produced by ANDing respective SPE, clock phase, and Read Enable signals, which yields a clock signal (READ(1) READ(2) READ(3), FIG. 5b) that controls the timing at which bits are latched out of the FIFO.

According to Parruck, a misalignment is detected and the corresponding values of the Read Enable signals are generated, using the J1 signals output by all of the FIFOs (of all of the terminating apparatus 10), Thus:

> "Misalignment (align error) can be defined logically as the state when for any particular J1, the logical AND of that J1 with clock #3 and with the opposite of the logical AND of each of the J1 signals is one. Logically:
>
> Misalignment=[J1OR] AND [J1AND] AND [CLOCK 3]
>
> where J1OR=[J1[l]] OR [J1[2]] OR . . . OR [J1[n]] and
>
> where J1AND=[J1[1]] AND [J1[2]] AND . . . AND [J1[n]].
>
> In other words, whenever one of the J1 values is high, if the all of the J1 values are not high together at clock 3, there is a misalignment" (col. 12, line 58-col 13, line5)

According to Parruck, detection of a misalignment causes the respective Read Enable signal of the misaligned data stream to go low (see FIG. 5c), which forces a corresponding gap in the FIFO read signal (READ(3), FIG. 5c) This gap causes a previous byte to be re-read from the FIFO, which corrects the misalignment. (col. 13, lines 40-54). It will be noted, however, that this operation cannot involve controlling the position of the read pointer, because Parruck concludes his discussion of realignment by stating that "the pointers on the register banks of the FIFOs are realigned such that the read pointer is half a FIFO away from the write pointer; i.e, the FIFO is reset to a depth of fifteen bytes." [col. 13, lines 64-68]. Clearly, if the data stream realignment system relied upon controlling the position of the read pointer, re-adjusting that position to "half a FIFO away from the write pointer" would negate the realignment function.

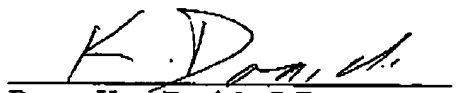
Thus it will be seen that Parruck teaches directly away from the claimed feature of controlling "a position of a read pointer for reading the buffered first data stream based on a selected one of the local and master strobe signals" as required by the present invention. In particular, Parruck explicitly teaches that the read pointer is adjusted to be "half a FIFO away from the write pointer". As mentioned above, this inherently precludes controlling the read pointer for any other purpose, and in any event, the adjustment is based on a desired FIFO fill, not a strobe signal.

Previous claims 1, 19 and 39 required that position of the read pointer is controlled using " a selected one of the local and master strobe signals". Implicit in this statement is the requirement that it be possible to make a selection, as is described in the original specification. Claims 1, 19 and 39 have been amended to make this requirement explicit. Thus claims 1 and 19 now require" a switch circuit adapted to select one of the local and master strobe signals ", while claim 39 defines a step of " selecting one of a local strobe signal and the master strobe signal". This feature is believed to provide further grounds for patentability over Parrcuk, because Parruck clearly fails to teach or fairly suggest any equivalent. In that respect, Parruck teaches that realignment of the data streams is accomplished using the J1 signal. To the extent that the J1 signal can be equated to the local strobe of the present invention, Parruck does not provide any other signal that may serve as the master strobe, and further provides no means by which it is possible to select a strobe signal from among a pair of signals for use in realigning the data streams. None of the other known prior art supplies the missing teaching.

In light of the foregoing, it is respectfully submitted that the presently claimed invention is clearly distinguishable over the teaching of the cited references, taken alone or in any combination. Thus it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 19-5113.

Respectfully submitted,



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